Study on Thermal Simulation and Verification Method for Ceramic Packaging Chips

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Abstract: In this paper, the DELPHI thermal transfer route was studied by simulation based on a kind of self-designed ceramic packaging chip. The influence of environment temperature on junction temperature and thermal resistance was studied by infra-optical test method and electrical test method. The results showed that, the junction temperature increased from 28.5℃ to 134.5℃ and the thermal resistance increased from 1.850℃/W to 2.782℃/W while the environment temperature increased from 25℃ to 125℃. The thermal resistance increased with the increases of environment temperature and the junction temperature. Furthermore, the high temperature zone existed near the local power consumption unit, leading to the failure of the device. In this study, the environment temperature on the distribution of internal temperature field of the chip was systematically analyzed. The infra-optical method was compared with the electrical method and the reason for the tolerance between the simulation and test is investigated. This study lays the foundations for the thermal reliability and failure analysis of ceramic chips and could be reference for thermal properties study in practical work.

1. Introduction

Temperature is an important factor for reliability of electronic devices. About 55% electronic equipment was failure related to the temperature [1]. The work temperature requirements of the general civil level electronic components is 0-70 ℃, industrial-grade is: -40-85 ℃, the military level is: -55-128 ℃. With electronic power increasing, the environmental requirement for application is more and more complex, ceramic packaging electronic components with good thermal reliability has been applied in automotive electronics, aerospace and other areas [2]. Junction temperature and thermal resistance of semiconductor device are considered as the critical parameters for reliability device performance and lifetime. There are two kinds of testing methods, which is infra-optical test method and electrical test method. Infra-optical test method could directly capture junction temperature Rth by removing the cap of the shell or head. Electrical test method is to determine Rth indirectly by testing the active layer of p-n junction voltage and the diode junction

temperature of integrated circuit substrate [3]. Infra-optical method belongs to the non-contact temperature measuring method, will not cause damage to the device [4]. In this paper, The DELPHI thermal resistance model was studied by simulation based on a ceramic packaging DSP chip. The main thermal transfer route was junction to bottom of housing. The influence of environment temperature on junction temperature and thermal resistance was studied by infrared optical method. The results showed that, the junction temperature increased from 28.5° C to 134.5° C and the thermal resistance increased from 1.850° C /W to 2.782° C /W while the environment temperature increased from 25° C to 125° C. The thermal resistance increased due to decrease of thermal conductivity and increase of junction temperature and total device temperature. Furthermore, the high temperature zone existed near the local power consumption unit, leading to the failure of the device. The infra-optical method was compared with the electrical method and infra-optical method was more accurate and reliable. The deviation between simulation and electrical method was due to the ideal simulation model and structure model, and the tolerance inside the chip during manufacturing. This study lays the foundations for the thermal reliability and failure analysis of ceramic chips and could be reference for thermal properties study in practical work.

2. Structure Modeling and Thermal Model Analysis

2.1. Structure of the Device and Finite Element Modelling

The finite element method software ANSYS was utilized to model the self-designed ceramic packaging chips. The internal structure of the chip is depicted in Figure.1, which contained cover, housing, seal ring, bonding wires, die, bonding plies and pins. The size and the thermal conductivity of the parts are shown in Table 1. Due to the higher thermal conductivity of ceramic housing and the relatively thinner bonding wires, the influence of the bonding wires on thermal transmission was slight, therefore, the bonding wires could be ignored during study

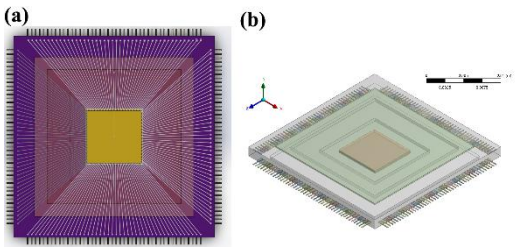


Figure 1: 3D structure model for DSP chips based on ceramic package
(a) top view (b) axonometric view.

Table 1: Parameters of materials for simulation.

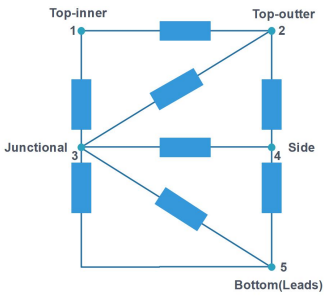
Material	Size/mm	Thermal conductivity /W • (m° C)-1
Kovar alloy	19×19×0.2	17.0
Ceramics	24×24×0.5	16.7
Sillicon	6.9×6.1×0.35	150(T/300)-1.3
Conductive adhesive	6.9×6.1×0.1	2.5
Si-Al bonding wire	ϕ0.031	230
Gold over nickel	Width of 0.2	90

The chip followed the energy conservation equation during thermal transmission process, thus the electric power of the chips equals the heat flow released by convection and heat conduction.

$$\rho c_p[\frac{\partial \theta}{\partial t}+\upsilon\nabla\theta]=\nabla(k\nabla\theta)-\frac{2}{3}\mu(\nabla\upsilon)^2+2(\mu s\cdot s)+\beta\theta\frac{\mathrm{d}\rho}{\mathrm{d}t} \quad (1)$$

The physical model of thermal characteristics included thermal resistance network model and finite element model. The thermal resistance network model includes linear thermal resistance network model, star thermal resistance network model and DELPHI thermal resistance network model. DELPHI thermal resistance network model, the most advanced model, was adopted in our study. The thermal transmission route is shown in Table 2. The thermal node of the top included two parts. Top-inner indicated the cover node of the top, while the top-outer indicated the ceramic housing node of the top (on the outer of the top). Junctional indicated the node of the junction temperature. Side indicated the node of the side of the ceramic housing while Bottom indicated the bottom of the ceramic housing that was in contact with the pins. The thermal transmission routes were seven in total. The internal heat source of the chip was 16.66×10-2W/mm3, which was equivalent to power dissipation of 2.696W. The heat convection coefficient of the air was set as 25W/(mm2·°C).

Table 2: Thermal transfer route for DSP chips.

DELPHI model of the chip	No.	Thermal transmission route
	A	Junction(3)→Top-inner(1)
	B	Junction(3)→Top-outer(2)
	C	Junction(3)→Top-inner(1)→Top-outer (2)
	D	Junction (3)→Side(4)
	E	Junction (3)→Bottom(5)
	F	Junction (3)→Leads(5)

2.2. Simulation Results and Analysis

The simulation results of the chip at the ambient temperature of . 25.0° C, 65.0° C and 125.0° C are shown in Figure 2. The temperature distribution curves were fitted by linear function, where D indicated the distance from bottom of the housing to the top of the chip.

Temperature distribution at 25° C:

$$\begin{aligned} t &= 2.238x+24.98(0<x<1) \\ t &= 16.95x+10.59(1<x<1.1) \\ t &= 0.16x+29.27(1.1<x<1.45) \end{aligned} \quad (2)$$

Temperature distribution at 65° C:

$$t = 2.25x+64.98(0<x<1)\ t = 17.15x+110.40(1<x<1.1)$$
$$\begin{aligned} t &= 17.12x+50.43(1<x<1.1) \\ t &= 0.23x+69.22(1.1<x<1.45) \end{aligned} \quad (3)$$

Temperature distribution at 125° C:

$$t = 2.26x+124.98(0<x<1)$$

$$t = 0.27x+129.26(1.1<x<1.45) \quad (4)$$

The junction of the die was 29.489° C at the ambient temperature of 25° C, while that of the bonding plies and the bottom of the housing was 27° C and 25° C. In addition, other part of the

housing and cover was 25° C. It is revealed that the valid thermal transmission route was Route E. Hence, the thermal resistance analyzed in our study was junction-bottom thermal resistance. The discrepancy between ambient temperature and junction temperature increased slightly with increase of ambient temperature.

There exists some tolerance between simulation results and reality due to the difference of finite element modeling and parameter settings.

Table 3: Simulation result with different ambient temperature.

Ambient temperature° C	Junctional tempature° C	Case temperature° C	Thermal resistance° C /W
25.0	29.489	25.0	1.665
65.0	69.515	65.0	1.674
125.0	129.55	125.0	1.687

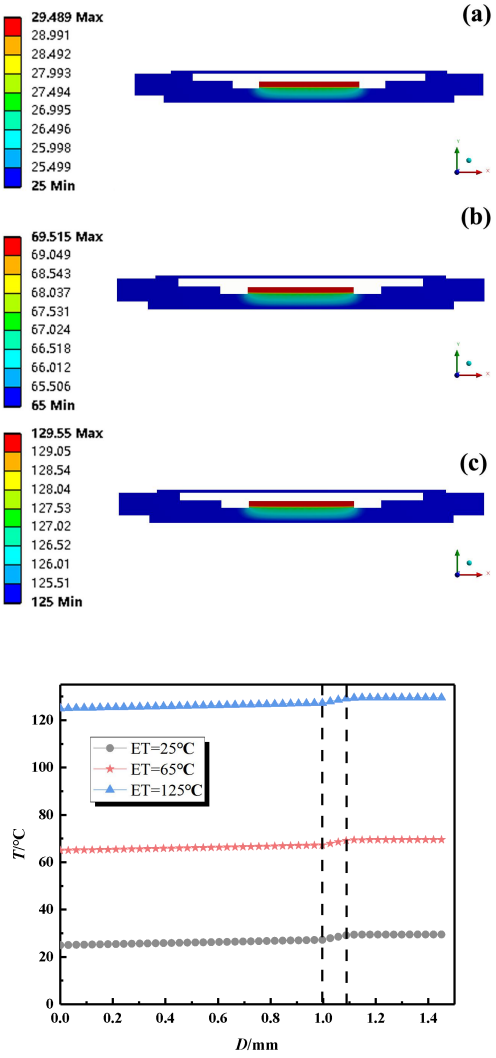


Figure 2: Thermal stress distribution at ambient temperature of (a)25℃ (b) 65℃ and (c) 125℃ for chips.

3. Experimental Results and Analysis

Infra-optical test method was utilized to study the influence of ambient temperature on junction temperature and thermal resistance. The temperature of the housing bottom of the chip was measured before unsealing and the temperature of the die was measure by infra-optical test system after unsealing and electrification of the chip. The test system is shown in Figure 3.

Figure 3: Infrared-optical measurement and data process system.

3.1. Thermal Characteristics of the Chip

Table 4: Comparation for Thermal Resistance Test.

Ambient temperature (℃)	Junction voltage （V）	Case temperautre (℃)	Average junction temperautre(° C)	Average Thermal resistance (℃/W)
25.0	0.545	25.7	28.5	1.850
45.0	0.496	46.5	52.1	2.077
65.0	0.459	68.2	74.0	2.151
85.0	0.418	86.5	92.5	2.226
105.0	0.376	108.3	114.7	2.373
125.0	0.332	127.0	134.5	2.782

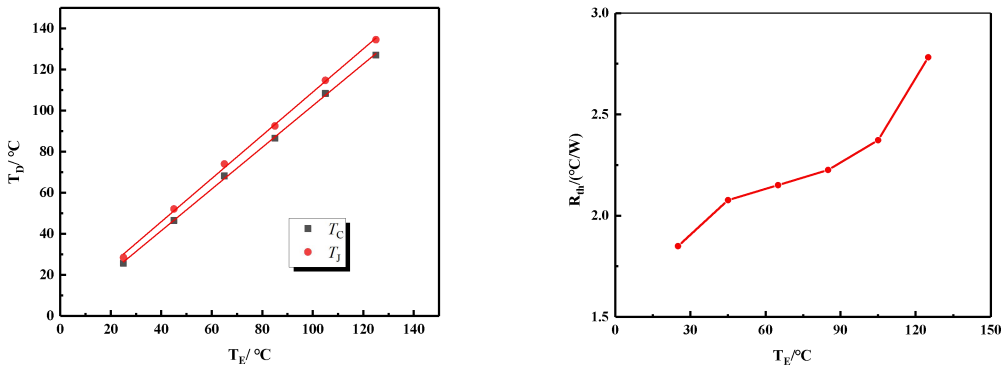


Figure 4: Change curves of junction temperature, shell temperature and thermal resistance under different ambient temperature.

The junction temperature (TJ), case temperature (TC) and thermal resistance (Rth) of the chip at various ambient temperature (TE) were shown in Figure 4 and Table 4 The junction temperature of the chip increased from 28.5 ° C to 135.0 ° C, the junction voltage decreased from 0.545V to

0.332V and the thermal resistance increased from 4.85° C/W to 5.25° C/W with increase of ambient temperature from 25° C to 125° C.

The thermal resistance is normally regarded at a constant that is fixed with the change of the environment parameters. However, in our study, the thermal resistance increased by 12.3% with increase of ambient temperature from 25° C to 45° C, while it increased by 17.2% with increase of ambient temperature from 105° C to 125° C. The influence of thermal effect of the device on thermal resistance and junction temperature of the device intensified. Firstly, the increase of ambient temperature could lead to the decrease of the thermal conductivity. Chen's study showed that the thermal conductivity of the die decreased from 884W/(m • K) at 100K to 61.9W/(m • K) at 600K. Christensen found that the thermal conductivity of GaN chip decreased from 250W/(m • K) at 25° C to 175W/(m • K) at 175° C. The decrease of thermal conductivity could result in poor heat conduction performance, therefore, the thermal resistance showed increasement. Secondly, the temperature of the chip (the initial value equals the ambient temperature) increased with increase of ambient temperature, leading to the poor heat dissipation effect. Thus, heat aggregated easily inside the chip, which showed the increase of thermal resistance. Additionally, the junction temperature (the initial value equals the ambient temperature) also increased with increase of ambient temperature. As shown in Tab.4, the junction temperature reached 134.5° C at the ambient temperature of 125° C. The combined effect of increment of junction temperature and poor abilities of thermal conduction might lead to the aggravated increment of junction temperature. In this condition, thermal failure of the chip was more easily observed.

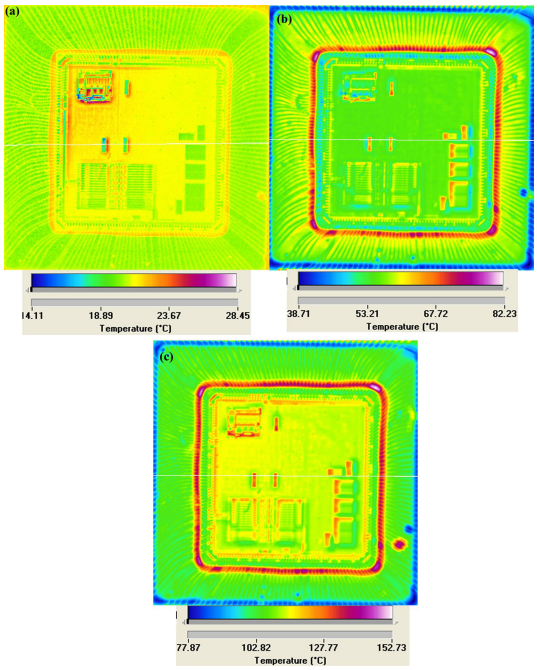


Figure 5 Thermal stress distribution at ambient temperature of
(a) 25℃ (b) 65℃ (c) 125℃ for infrared Scope.

Figure 5 showed the thermal field distribution of the chip at various ambient temperature. It is revealed that the temperatures of special structure units inside the die were 28.5° C, 82.2° C and 152.2° C at ambient temperature of 25° C, 65° C and 125° C, respectively. Thus, the thermal resistance of the chip was conditional. The added condition included the ambient temperature.

3.2. Comparision Infrared Optical Method with Electrical Method and Simulation

The electrical method was utilized to study the thermal characteristics of the chip. The structure function was deduced by mathematical operations on the chip temperature vs. time curves. As shown in Fig.6, the thermal resistance was 2.120 ° C/W at ambient temperature of 65 ° C via electrical method measurement. The comparisons of the three methods were shown in Tab.5. The thermal resistance of the chip increased from 2.050 ° C/W to 2.60 ° C/W and the junction temperature increased from 30.5° C to 132.5° C with increase of ambient temperature from 25° C to 125 ° C. The little tolerance between the results of electrical method and results of infrared optical method may be due to that the junction temperature via electrical method was average values while the junction temperature via infrared optical method was the temperature inside the die. Thus, the junction temperature via infrared optical method was more accurate and reliable. The results of simulation method and electrical method exhibited the same qualitative regularity, i.e. the thermal resistance increased with increase of ambient temperature. However, the deviation was about 30%, which was due to the ideal simulation model and structure model, and the tolerance inside the chip during manufacturing.

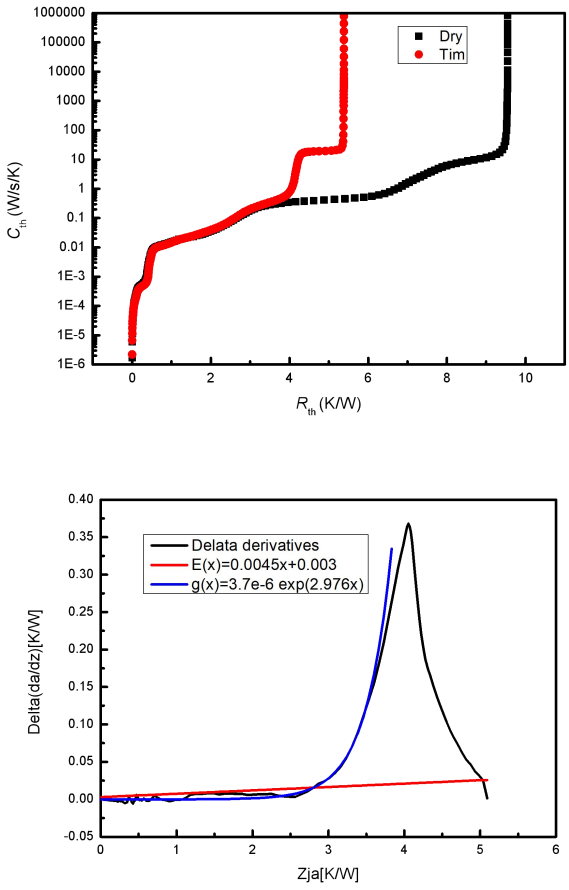


Figure 6: Thermal Resistance Test result for electronic measurement at ambient temperature of 65℃.

Table 5: Test result compared by Infra-scope and electronic measurement.

Ambient temperature(°C)	Electrical test		Infra-optical test		Simulation	
	TJ (°C)	Rth (°C/W)	TJ (°C)	Rth (°C/W)	TJ (°C)	Rth (°C /W)
25.0	30.5	2.050	28.5	1.850	29.5	1.665
65.0	72.8	2.120	74.0	2.151	70.9	1.674
125.0	132.5	2.60	134.5	2.782	130.2	1.687

4. Conclusions

The DELPHI thermal resistance model was studied by simulation based on a ceramic packaging DSP chip. The main thermal transfer route was junction to bottom of housing The influence of environment temperature on junction temperature and thermal resistance was studied by infrared optical method. The results showed that, the junction temperature increased from 28.5 ° C to 134.5 ° C and the thermal resistance increased from 1.850 ° C /W to 2.782 ° C /W while the environment temperature increased from 25° C to 125° C. The thermal resistance increased due to decrease of thermal conductivity and increase of junction temperature and total device temperature. Furthermore, the high temperature zone existed near the local power consumption unit, leading to the failure of the device. The infra-optical method was compared with the electrical method. And infra-optical method was more accurate and reliable. The deviation between simulation and electrical method was due to the ideal simulation model and structure model, and the tolerance inside the chip during manufacturing. This study lays the foundations for the thermal reliability and failure analysis of ceramic chips and provides reference points for the thermal properties study in practical work.

Acknowledgments

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